

3.3V 5V \pm 12V Housekeeping IC

- Over voltage and under voltage protection for 3.3V 5V and \pm 12V without external components
- Under voltage blanking function
- Power good input/output
- Externally adjustable PG delay
- Fault output
- Remote input
- Externally adjustable remote delay
- Precision voltage reference
- 2kV ESD protection (HBM)

Description

The TSM114 integrated circuit incorporates all of the sensing circuitry required to regulate and protect a multiple-output power supply (3.3V, 5V, and \pm 12V) from both over-voltage and under-voltage.

The TSM114 also includes all of the necessary functions for housekeeping features, which allow for safe operation under all conditions, as well as very high system integration.

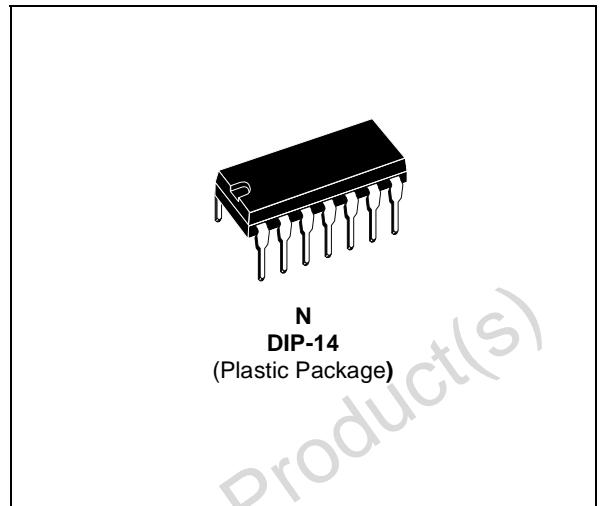
A precise voltage reference is also integrated in the TSM114

Applications

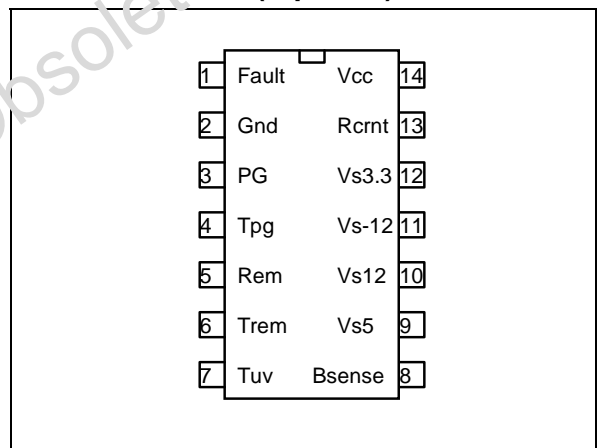
- PC SMPS multiple Power Line Housekeeping IC (3.3V 5V \pm 12V)

Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
TSM114IN	0 to +95°C	DIP14	Tube	TSM114



Pin Connections (top view)



1 Pin Descriptions

Table 1: This table gives the pin description for DIP14 package

Name	Pin #	Type	Function
Fault	1	Open collector	Fault output. Output of the over voltage and under voltage comparators
Gnd	2	Power supply	Signal ground and silicon substrate
PG	3	Open collector	Output of the Tpg comparator. This pin goes low upon an under voltage condition. Except for the delay set by the Tpg capacitor this pin always reflects the actual state of the under voltage sensing comparators output.
Tpg	4	Timing capacitor	A capacitor from this pin to Gnd provides a delay between outputs rail voltage within regulation and PG output going high. Capacitor discharges whenever Bsense low or Rem high or UVP is detected.
Rem	5	Control Input pin	Pulling this pin high will send the Fault pin high latching off the power supply, reset the internal latch, discharge the start-up timing capacitors, Tuv and Tpg capacitors, allowing normal start up of the system. Pulling this pin low will send the Fault pin low, initiating a normal start up function.
Trem	6	Timing capacitor	A capacitor from this pin to Gnd will delay the Fault signal when the Rem pin is used to shut down the power supply. The PG will signal a power failure warning immediately, but the Fault pin shut down of the power will be delayed.
Tuv	7	Timing capacitor	A capacitor from this pin to Gnd will provide the under voltage blanking function. This capacitor is charging when the Bsense and Rem signal is in the right state. As the voltage at this pin is larger than the Vref voltage. The under voltage function resume.
Bsense	8	Control input pin	Non inverting input to the Bsense voltage sensing comparator. Pulling this pin lower than 2.5V will cause PG goes low and Tuv goes low.
Vs5	9	Analog input	Over voltage and under voltage detection for +5V rail
Vs12	10	Analog input	Over voltage and under voltage detection for +12V rail
Vs-12	11	Analog input	Over voltage and under voltage detection for -12V rail.
Vs3.3	12	Analog input	Over voltage and under voltage detection for 3.3V rail. This function is disabled by connecting to Vcc
Rcrnt	13	Analog input	A resistor from this pin to Gnd will provide the internal constant current.
Vcc	14	Power supply	Supply input voltage

2 Absolute Maximum Ratings

Table 2: Key parameters and their absolute maximum ratings

Symbol	DC Supply Voltage	Value	Unit
Vcc	DC Supply Voltage ¹	-0.3 to 25	V
Vpmax	Terminal voltage V12, V5, V3.3	-0.3 to 25	V
Vnmax	Terminal voltage V-12	-16 to Vref	V
VDBTT	VTuv, VTpg, VTrem input voltage	-0.3 to 3.3V	V
VTER	Other terminals	-0.3 to Vcc	V
PT	Power dissipation	1	W
Tooper	Operational temperature	0 to 95	°C
Tstg	Storage temperature	-55 to 150	°C
Tj	Junction temperature	150	°C
ESD	Electrostatic Discharge	2K	V

1) All voltage values, except differential voltage are with respect to network ground terminal.

Table 3: Operating Conditions

Symbol	Parameter	Value	Unit
Vcc	DC Supply Conditions	4.2 to 24	V

3 Electrical Characteristics

Table 4: T_{amb} = 25°C, V_{cc}=5V, V_{s3.3}=1.3V, V_{s5}=5V, V_{s12}= 12V, V_{s-12}=-12V, Rem=Low, R_{crnt}=24KΩ

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Total Current Consumption						
I _{cc}	Total Supply Current		4	6	8	mA
V _{ccmin}	Min operating V _{cc}				4.2	V
Over Voltage and Under Voltage Protection						
V _{ov12}	Over Voltage Sense 12V		13.5	14	14.4	V
V _{uv12}	Under Voltage Sense 12V		8.85	9.12	9.39	V
I _{in12}	Input current Voltage sense 12V		100	200	300	μA
V _{ov5}	Over Voltage Sense 5V		6.01	6.20	6.39	V
V _{uv5}	Under Voltage Sense 5V		4.00	4.12	4.24	V
I _{in5}	Input current Voltage Sense 5V		100	200	300	μA
V _{ov3.3}	Over Voltage Sense 3.3V		1.43	1.475	1.52	V
V _{uv3.3}	Under Voltage Sense 3.3V		1.09	1.125	1.16	V
I _{in3.3}	Input current Voltage Sense 3.3V		-2	0	2	μA
Dis3.3	Disable Voltage Sense 3.3V ¹		3.0	3.3	4.0	V
V _{ov-12}	Over Voltage Sense -12V		-15.49	-15.04	-14.58	V
V _{uv-12}	Under Voltage Sense -12V		-9.99	-9.70	-9.39	V
I _{in-12}	Input current Voltage sense -12V		-300	-200	-100	μA
Dis-12	Disable Voltage Sense -12V		1.5	2	2.5	V
T _{delay}	Internal time		18	30	42	μs
Bsense						
Th _{bs}	Bsense voltage threshold		2.43	2.50	2.562	V
I _{lbs}	Bsense current leakage		-1.2	0		μA
I _{obs}	Current source	Bsense=3V	225	250	275	μA
D _{lobsT}	Current source drift in temperature	T _{min} . < T _{amb} < T _{max}		10		μA
V _{bsoh}	Clamp voltage	I _{oBsense} =1μA	3.3	3.6	3.9	V
V _{inbs}	Input voltage		-0.3		3.3	V
Under Voltage Blanking (T_{uv})						
I _{otuv}	Current output source		9	10	11	μA
TH _{tuv}	High threshold blanking	From low to high voltage	2.425	2.50	2.575	V
TL _{tuv}	Low threshold blanking	From high to low voltage	1.9	2	2.1	V
I _{dtuv}	Current discharge of T _{uv}		2	5		mA
V _{tuvol}	Low output voltage				0.2	V
V _{tuvoh}	Clamp voltage		3.3	3.6	3.9	V
V _{inTuv}	Input voltage		-0.3		3.3	V
D _{lotuv}	Current source drift in temperature	T _{min} . < T _{amb} < T _{max}			2	μA
Rem						
TH _{rm}	High threshold	From Low to high	1.87	1.93	2.00	V
TL _{rm}	Low threshold	From high to low	1	1.2	1.4	V
TRem						
I _{otrm}	TRem current source		9	10	11	μA
TH _{trm}	High thresold voltage TRem	From low to high	2.425	2.50	2.575	V
TL _{trm}	Low thresold voltage TRem	From high to low	1.9	2	2.1	V

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Idtrm	Current discharge of TRem		2	5		mA
Vtrmol	Low output voltage				0.2	V
Vtrmoh	Clamp voltage		3.3	3.6	3.9	V
Vintrm	Input voltage		-0.3		3.3	V
Dlotrm	Current source drift in temperature	Tmin. < Tamb < Tmax			2	μA
Power Good (PG)						
Ipgol	Sink current	VoIPg=0.2V	10			mA
Vpgol	Low output voltage	Isink=10mA			0.2	V
Tpgr	Rise time PG	Rpg=1K			500	nS
Tpg						
Iotpg	Current source		9	10	11	μA
THtpg	High threshold	From low to high	2.425	2.50	2.575	V
TLtpg	Low threshold	From high to low	1.9	2	2.1	V
Idtpg	Current discharge		2	5		mA
Vtpgol	Low output voltage				0.2	V
Vtpgoh	Clamp voltage		3.3	3.6	3.9	V
Vintpg	Input voltage		-0.3		3.3	V
Dlotpg	Current source drift in temperature	Tmin. < Tamb < Tmax			2	μA
Fault						
Iftol	IFault sink current	VoIFault=0.2V	10			mA
Vftol	Low output voltage	IsinkFault=10mA			0.2	V
Rcrnt						
VRcrn	Output voltage		1.93	2.02	2.11	V

1) DisVs33 disable voltage shall be between 4V and Vcc. When using DisVs33 disable function, connected to Vcc is better.

Figure 1: Application Schematic

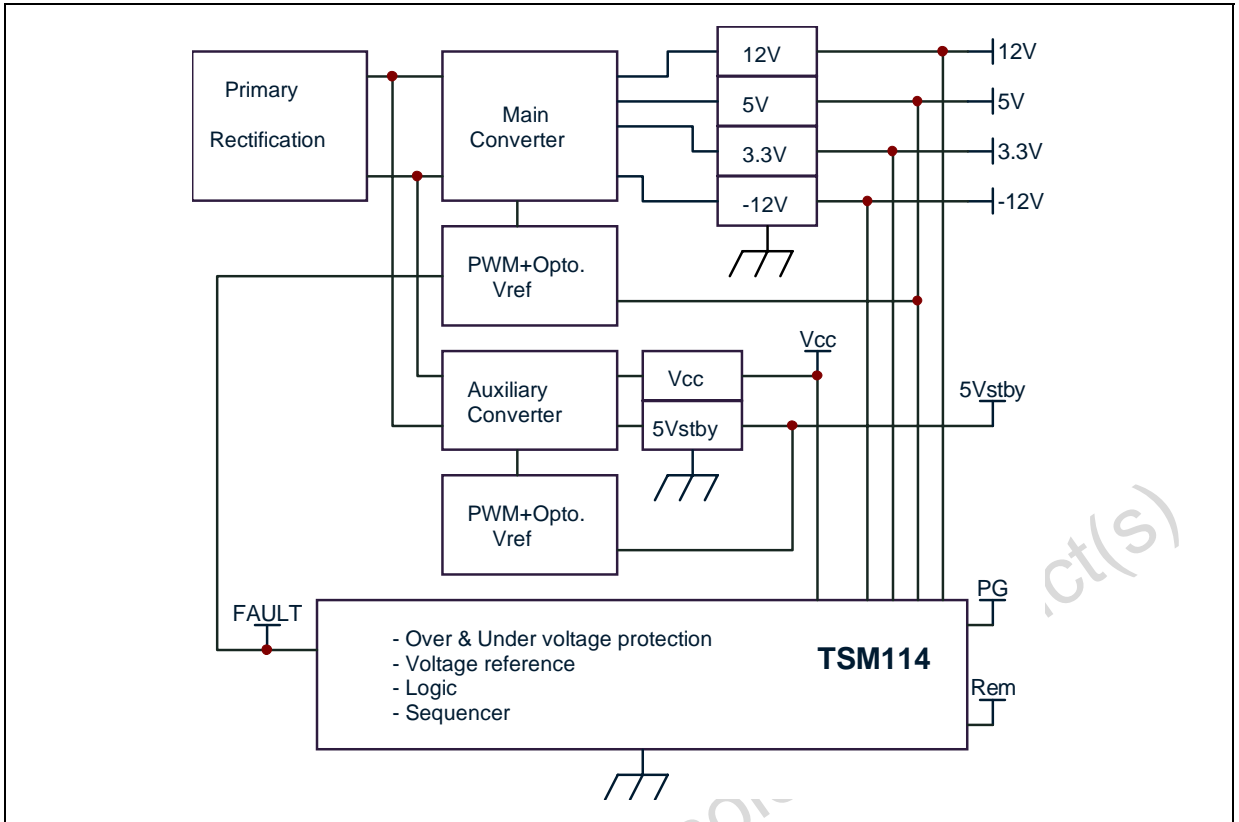


Figure 2: Internal Schematic

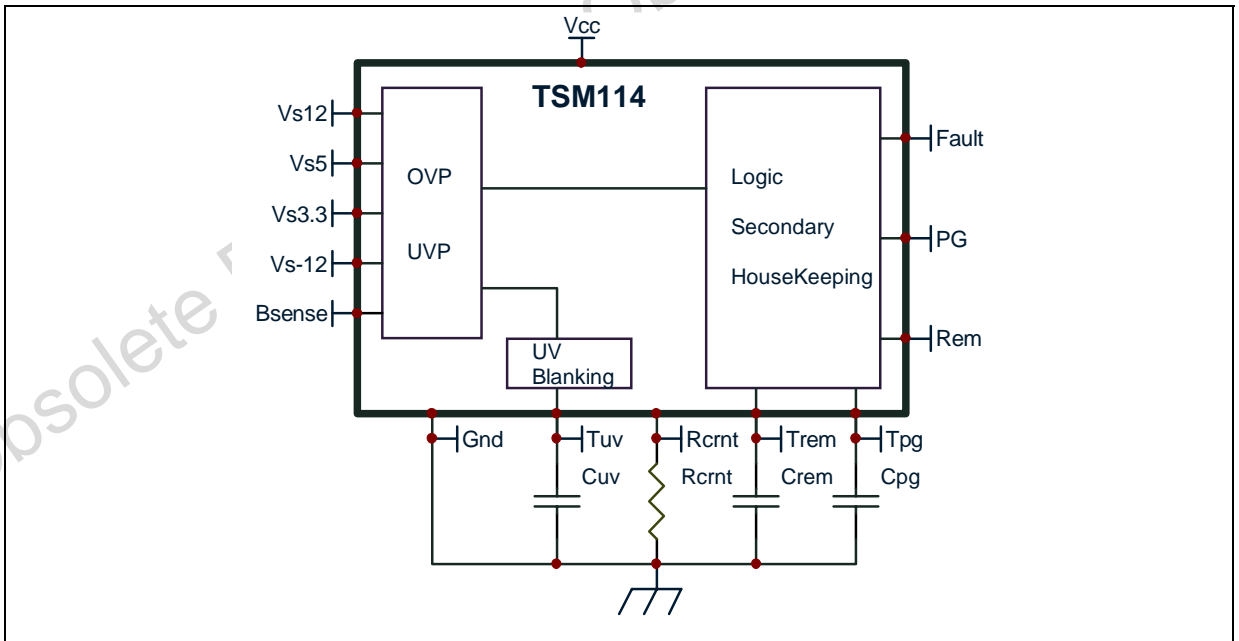
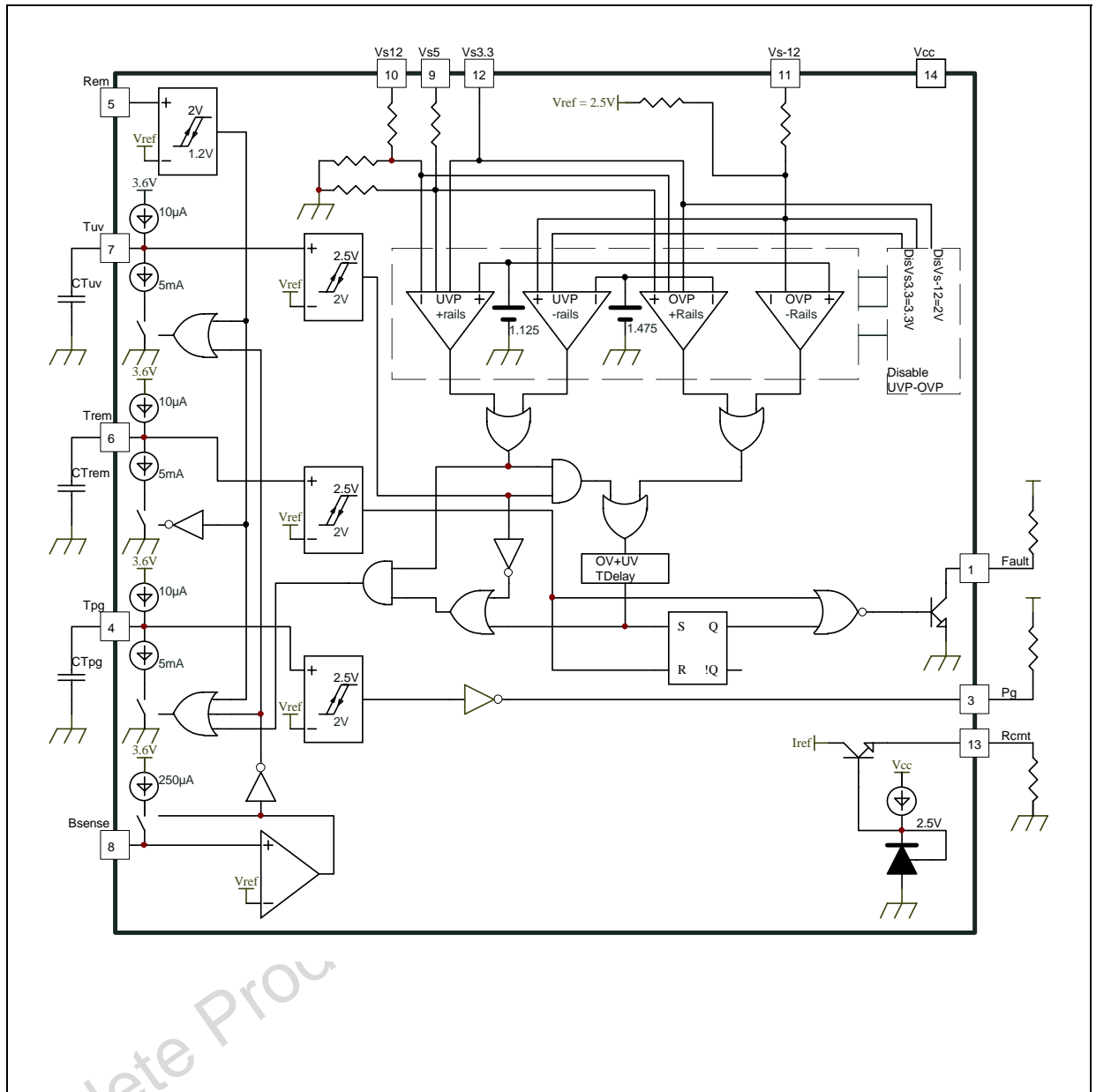


Figure 3: Detailed Internal Schematic



Obsolete Pro

Figure 4: Rem On/Off

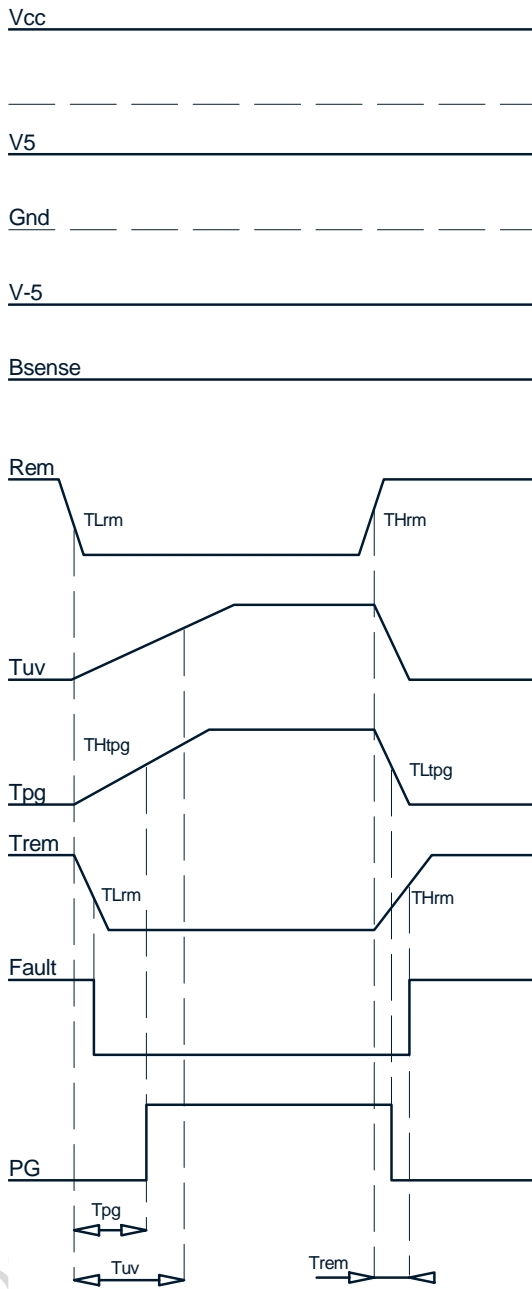


Figure 5: OVP Function Rem On/Off, Tuv start up

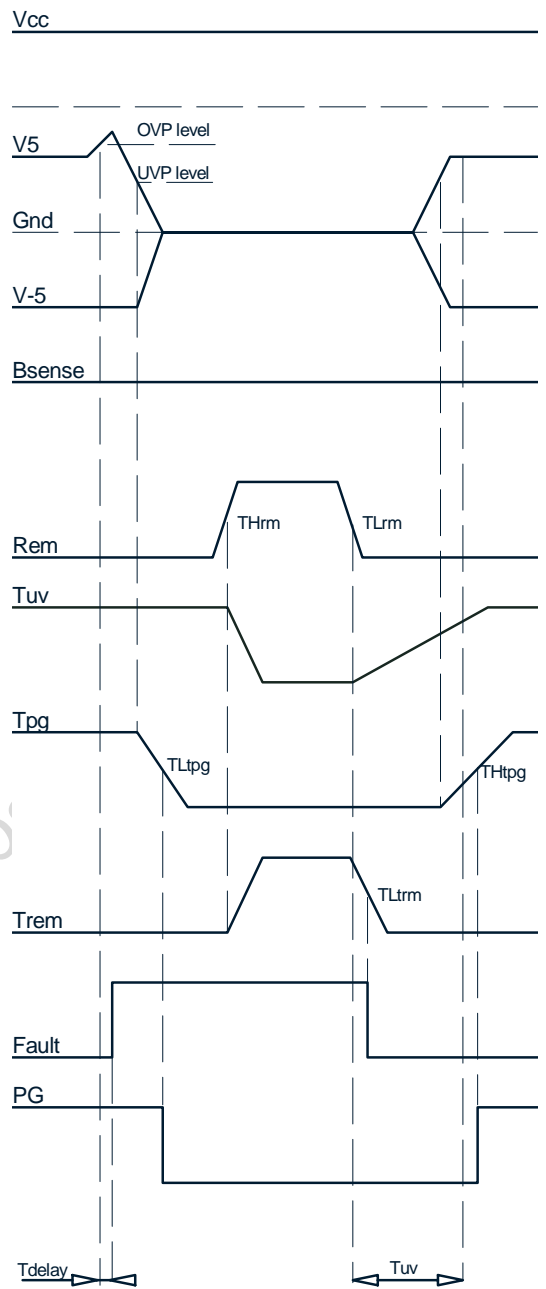


Figure 6: OVP function, Rem On/Off, Tuv start up

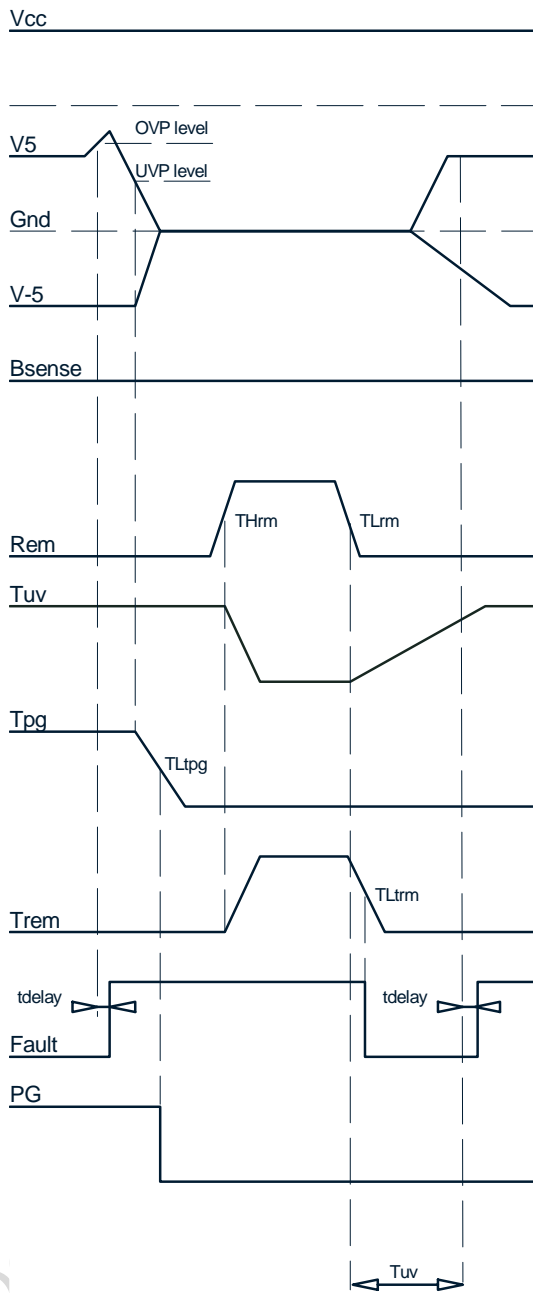


Figure 7: Vcc turn On/off, Bsense

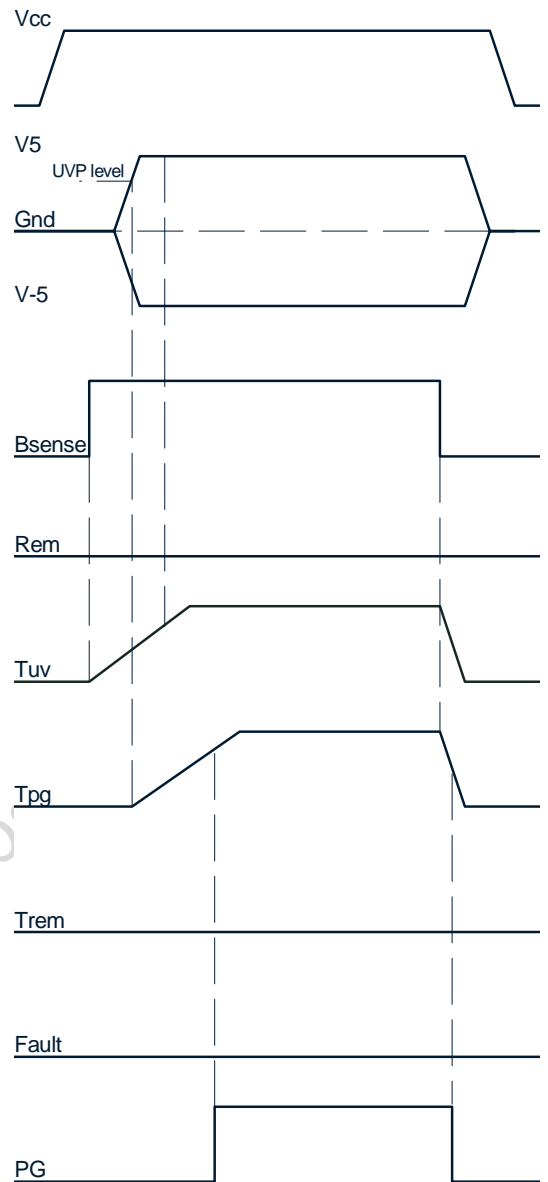


Figure 8: Vcc turn on, OVP function, Remote On/Off

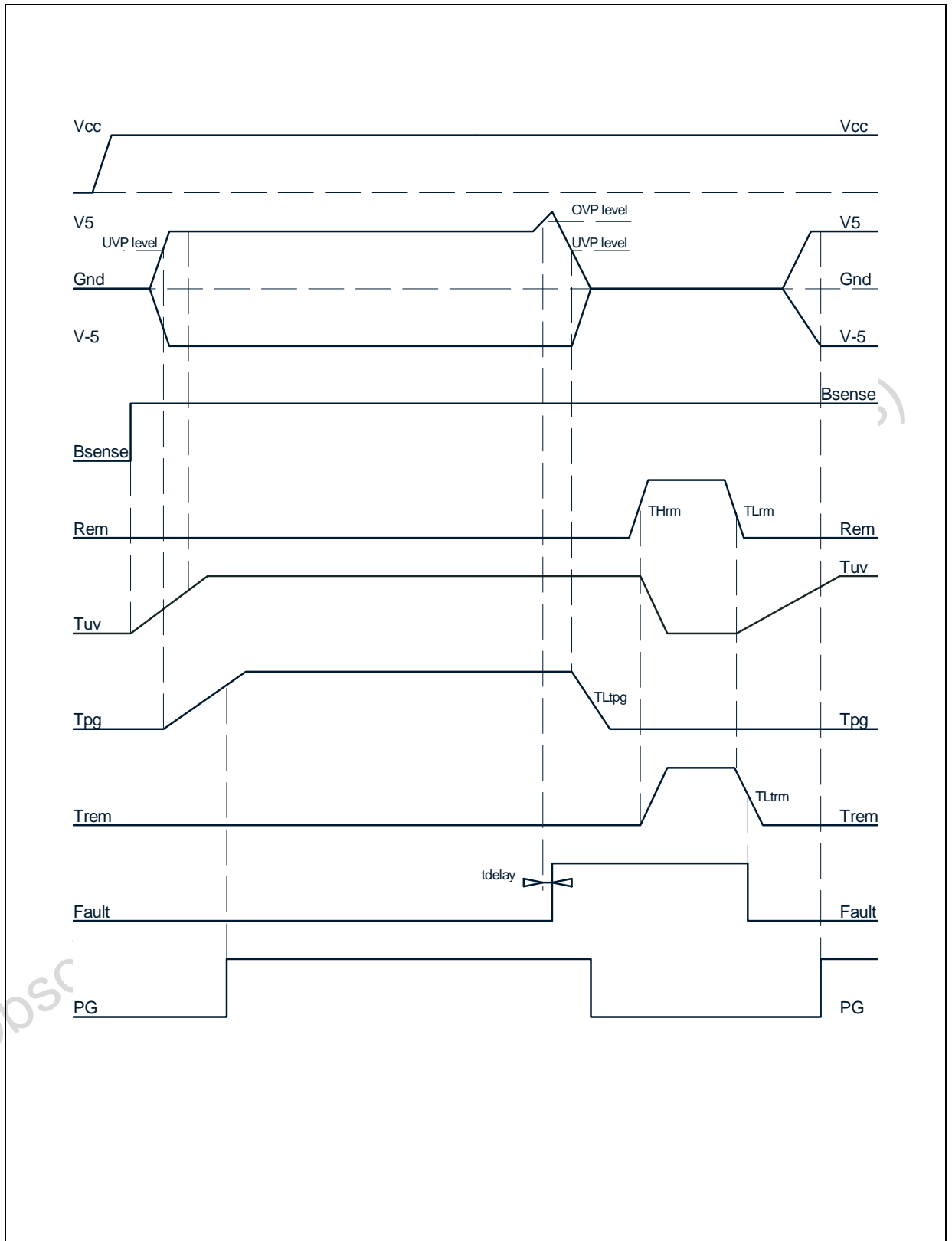


Figure 9: Vcc turn On, AC line reduce/resume Bsense

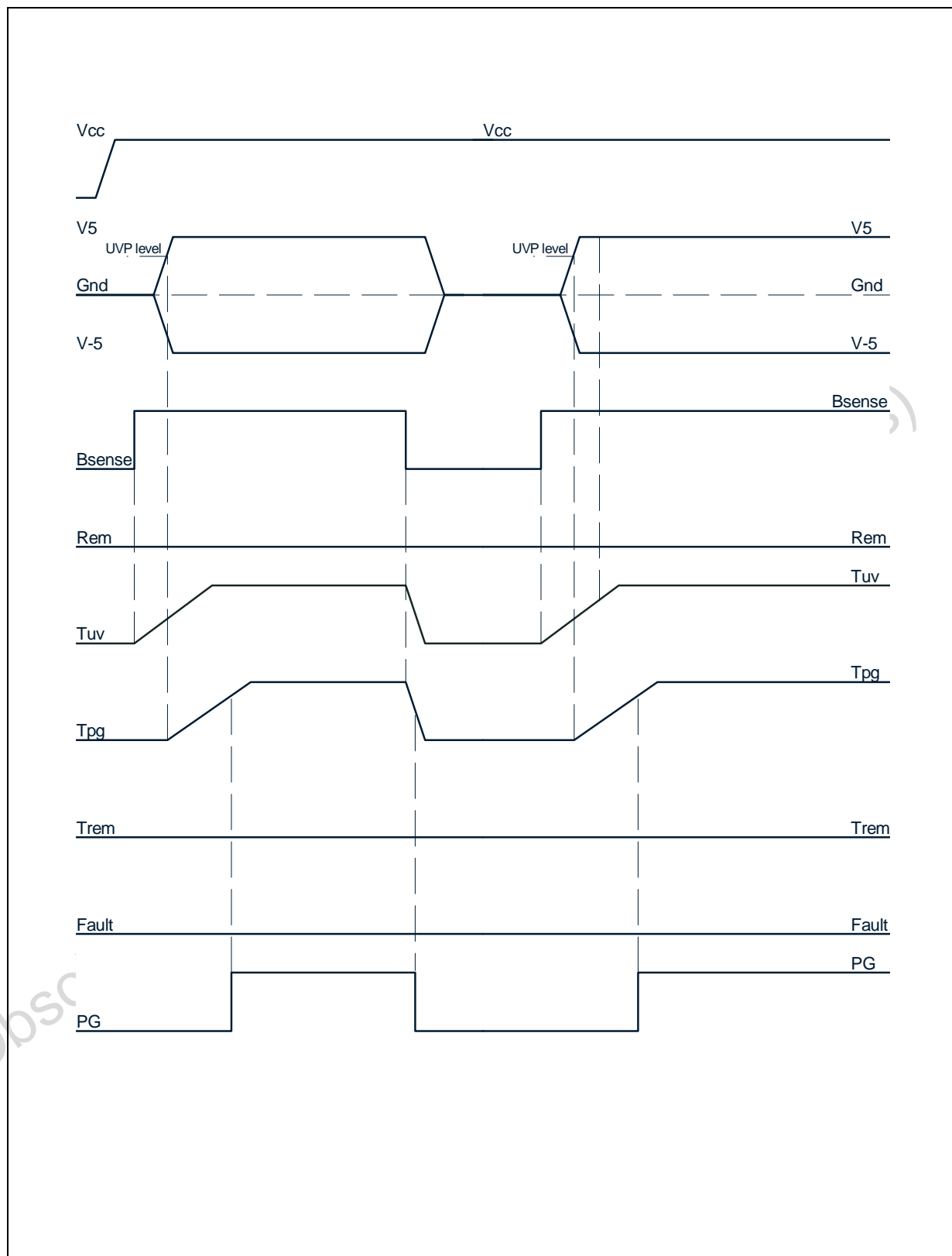


Table 5: Truth table for OVP and UVP detection

Vs12	Vs5	Vs3.3	Vs-12	Pg
$Uv < Vs_{12} < Ov$	$Uv < Vs_5 < Ov$	$Uv < Vs_{3.3} < Ov$	$Uv < Vs_{-12} < Ov$	1
Vuv12	x	x	x	0
Vov12	x	x	x	0
x	Vuv5	x	x	0
x	Vov5	x	x	0
x	x	Vuv3.3	x	0
x	x	Vov3.3	x	0
x	x	Dis3.3	x	Versus other rails
x	x	x	x	0
x	x	x	x	0
x	x	x	x	Versus other rails
x	x	x	Vuv-12	0
x	x	x	Vov-12	0
x	x	x	Dis-12	Versus other rails

4 Housekeeping IC

TSM114 is a one chip solution for all PC SMPS: it integrates on one chip the Housekeeping Circuitry (Over Voltage and Under Voltage protections, with adequate sequencing).

Multiple Power Line Protection

The TSM114 Housekeeping Circuit is dedicated to 3.3V, 5V and $\pm 12V$ power lines protection. It integrates a Precision Voltage Reference, a multiple Over Voltage Protection Circuit and a multiple Under Voltage Protection Circuit as well as all the necessary logic and transient timing management circuits for optimal and secure communication with the motherboard, during start up, switch off and stabilized conditions.

Over Voltage Protection

The Over Voltage Protection Circuit is made of comparators with internal voltage thresholds which do not require any external components for proper operation. The outputs of these comparators are ORed.

Under Voltage Protection

The Under Voltage Protection Circuit is made of comparators with internal voltage thresholds which do not require any external components for proper operation. The outputs of these comparators are ORed, and blanked by an internal delay circuitry (Power Up Blanking - T_{uv}) which can be adjusted with an external capacitor (C_{uv}). This allows that during power up, the under voltage protection circuit is inhibited.

Fault

The Over Voltage and Under Voltage Circuits outputs are ORed before activating a latch. When activated, this latch commands the full switch OFF of the main power lines (3.3V, 5V, 12V) by an external link between the housekeeping and the primary PWM circuits via the main optocoupler or any other device.

Power Good

The Under Voltage Circuits are ORed to switch the Power Good output active (PG) to warn the motherboard that the voltage of at least one of the three power lines is out of range. The PG activation bears an internal T_{pg} delay circuitry which can be adjusted with an external capacitor (C_{pg}).

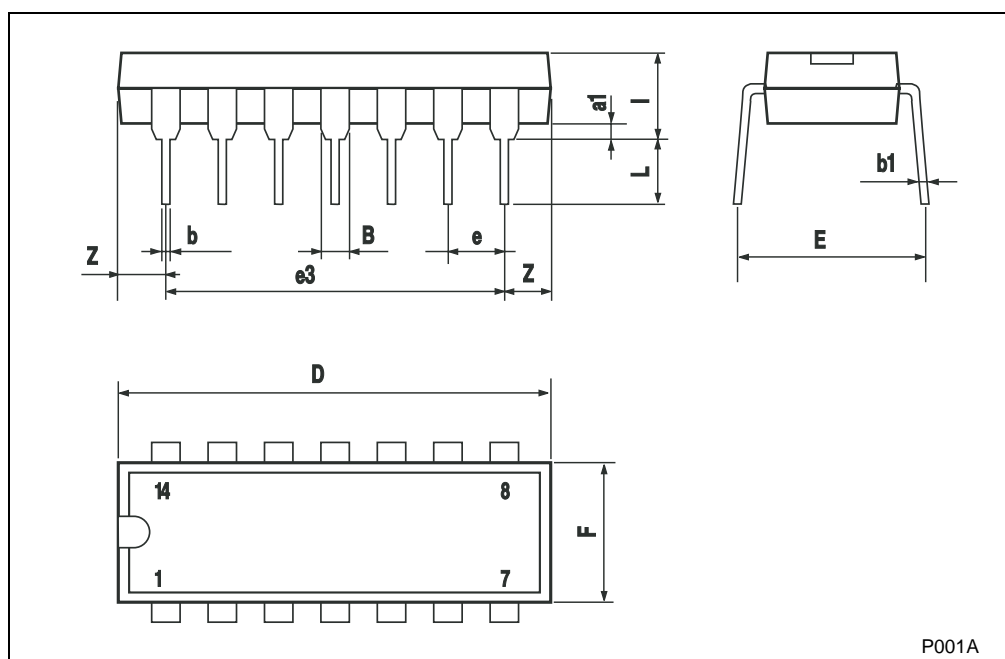
Remote Control

Thanks to this information link to the motherboard, a resetting signal to the latch is achievable with the Remote pin (REM). When the Remote pin is active, the external Fault link between Housekeeping circuit and the PWM generator is active (high = PWM OFF) and the PG pin is active (high). Note that to reset effectively the latch, a minimum width Remote pulse should be applied thanks to an internal delay circuitry (T_{rem}) which can be adjusted with an external capacitor (C_{rem}).

5 Package Mechanical Data

Plastic DIP-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



P001A

6 Revision History

Date	Revision	Description of Changes
01 October 2004	1	First Release

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics
All other names are the property of their respective owners

© 2004 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com